Menta Delivers Off-the-Shelf Embedded FPGA IP Cores that Enable a New Level of Flexibility to be built into Complex SOCs

New IP cores combined with EDA tools that simplify post-production customization

MONTPELLIER, France, September 9, 2015 — Menta SAS, a provider of embedded FPGA (eFPGA) Intellectual Property (IP), today announced a family of pre-defined off-the-shelf IP cores that enable a new level of flexibility to be built into next-generation complex System on Chip (SOC) devices. The new eFPGA IP cores, optimized for TSMC's 28 nanometer process, are combined with the company's proven Origami Programmer EDA tool that allows designers to make post-fabrication changes quickly and with ease.

Menta's complete solution addresses the overwhelming need for enhanced programmability of today's complex SOCs. Embedding an FPGA fabric as an IP core in into an SOC allows semiconductor designers and equipment manufacturers to update the silicon at will post production, thereby eliminating the cost and time associated with re-spinning silicon. Whether to implement a customer-specific feature, or a change to an evolving standard, Menta's solution allows designers to quickly and easily configure SOCs for a variety of defense, aerospace, automotive, industrial and consumer applications.

"Menta's goal is to make flexibility in SOC design a reality, while also delivering on the high density, low power and high speed required of parallel and co-processing used in today's complex designs," said Laurent Rougé, Founder and CEO of Menta. "The new off-the-shelf IP blocks make it easier than ever for designers to meet the demands of both increasing complexity with ever-shrinking time to market windows."

The family of IP cores includes six new eFPGA options that have from 4k-60k equivalent ASIC gates, plus DSP blocks. The IP cores are delivered as hard macros with optimized arrays sizes for the embedded logic blocks (eLB), embedded custom blocks (eCB), and embedded memory blocks (eMB), each of which are customizable in type, number and size to address various markets and applications. The eFPGA IP cores are designed for standard test compatibility with all common ASIC and SOC test solutions, featuring fault coverage up to 99.8% as announced earlier this year.

Menta's new off-the-shelf eFPGA IP cores are supplied with a proven EDA tool that supports design from HDL design to bitstream with synthesis, mapping, place and route. The enhanced eFPGA technology is based on Menta's proven Origami tool chains, which now include synthesis to allow RTL applications in VHDL, Verilog or SystemVerilog, as well as new SDC support for application design constraints. Additionally, new timing analyses tools enhance engineer
experience and facilitate designs.

Availability
Menta's new eFPGA IP cores and associated software are available now. For more information, please visit www.menta-efpga.com/technology, or contact our customer support team at info(at)menta-efpga.com.

About Menta
Menta is a privately held company based in Montpellier, France. The company provides embedded FPGA (eFPGA) technology for System on Chip (SoC), ASIC or System in Package (SiP) designs, from EDA tools to IP generation. Menta's programmable logic architecture is based on scalable, customizable and easily programmable architecture created to provide programmability for next-generation ASIC design with the benefits of FPGA design flexibility.
For more information, visit the company website at: www.menta-efpga.com