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Menta Offers Validation Board for Embedded FPGA Supporting TSMC's 28nm HPC+ Process

eFPGAs enable programmability in SoCs for mobile and consumer products

Austin, Texas, June 19, 2017 — Menta SAS, a provider of embedded FPGA (eFPGA) Intellectual Property (IP), today announced a validation board supporting TSMC's 28-nanometer High Performance Compact Plus (28HPC+) process. The board includes a test chip with an embedded FPGA (eFPGA) IP core from Menta, and is supplied with all of the hardware and software required for validation of the complete eFPGA design flow from RTL to bitstream, and through final hardware test and measurement. Menta's eFPGA technology will be demonstrated at booth #1329 this week at the Design Automation Conference in Austin, Texas.

Menta's eFPGAs enable programmability to be embedded into complex SoCs, allowing changes to be made to the RTL at will, post-production, thereby eliminating costly re-spins. This capability is critical to meeting the sometimes conflicting requirements of changing standards, security updates and shrinking time-to-market windows of mobile and consumer products, IoT devices, networking and automotive ICs.

"Menta is pleased to support TSMC's 28HPC+ process with a board that demonstrates Menta's eFPGAs and Origami Programmer software," said Vincent Markus, CEO of Menta. "This FPGA design, from PDK and standard cells libraries reception to GDSII tapeout, was complete in just two months which shows our ability to support different technology nodes with a very fast turnaround time."

The validation board includes all of the software and hardware necessary to implement the complete eFPGA design flow. In addition to the test chip with Menta's eFPGA, the board integrates a USB connector for bitstream programming, a microprocessor to manage bitstream signals with USB/FLASH/eFPGA, a 2Mb FLASH memory, design for test connectors, and a

standard 12V power supply.

Menta also provides customer support with Origami Programmer, a proven EDA tool that supports design from HDL design to bitstream with synthesis, mapping, place and route. Origami Programmer includes synthesis to allow RTL applications in VHDL, Verilog or SystemVerilog, as well as SDC support for application design constraints. Additionally, timing analyses tools enhance engineer experience and facilitate designs. The validation board demonstrates standard test compatibility with all common ASIC and SOC test solutions. Menta eFPGAs is unique in offering fault coverage greater than 99.6%.

Availability

Menta's eFPGA validation board, testchip, IP cores and associated software are available now. For more information, please visit www.menta-efpga.com, or contact our customer support team at info@menta-efpga.com.

About Menta

Menta is a privately held company based in Montpellier, France. The company provides embedded FPGA (eFPGA) technology for SoC, ASIC or SASSP designs. Menta's programmable logic architecture is based on scalable, customizable and easily programmable architecture created to provide programmability for next-generation ASIC design with the benefits of eFPGA design flexibility. For more information, visit the company website at: www.menta-efpga.com

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