eFPGA Core® IP

Embedded Field Programmable Gate Array IP

Menta® eFPGA Core® IP is based on a high-density embedded programmable logic architecture designed to be used in SoC, ASIC or ASSP. Using an eFPGA Core provides design flexibility and reduces time-to-market by enabling lifetime re-programmability. The technology allows logic to be changed after manufacturing, reduces the number of chip re-designs and amortizes chip development costs over several design derivatives. This is the ideal solution for semiconductor companies wanting to add configurability to their end products.

The Menta eFPGA Core IP integrates smoothly into any standard ASIC methodology and design flow. Available as a hard macro cell for high performance, low power and small die size solution, the eFPGA Core IP can be targeted to any silicon foundry (IDMs and pure-plays). Pre-defined eFPGA cores are readily available for fast delivery, or customers can choose to use the Menta Origami Designer™ environment to customize the eFPGA IP to customer requirements. Application mapping, configuration and place and route design steps are performed by Menta Origami Programmer™ tool suite, which is compatible with most third-party design entry, verification and test tools. Menta Origami Programmer™ is also used to generate the eFPGA bitstream files for post-manufacturing programming.
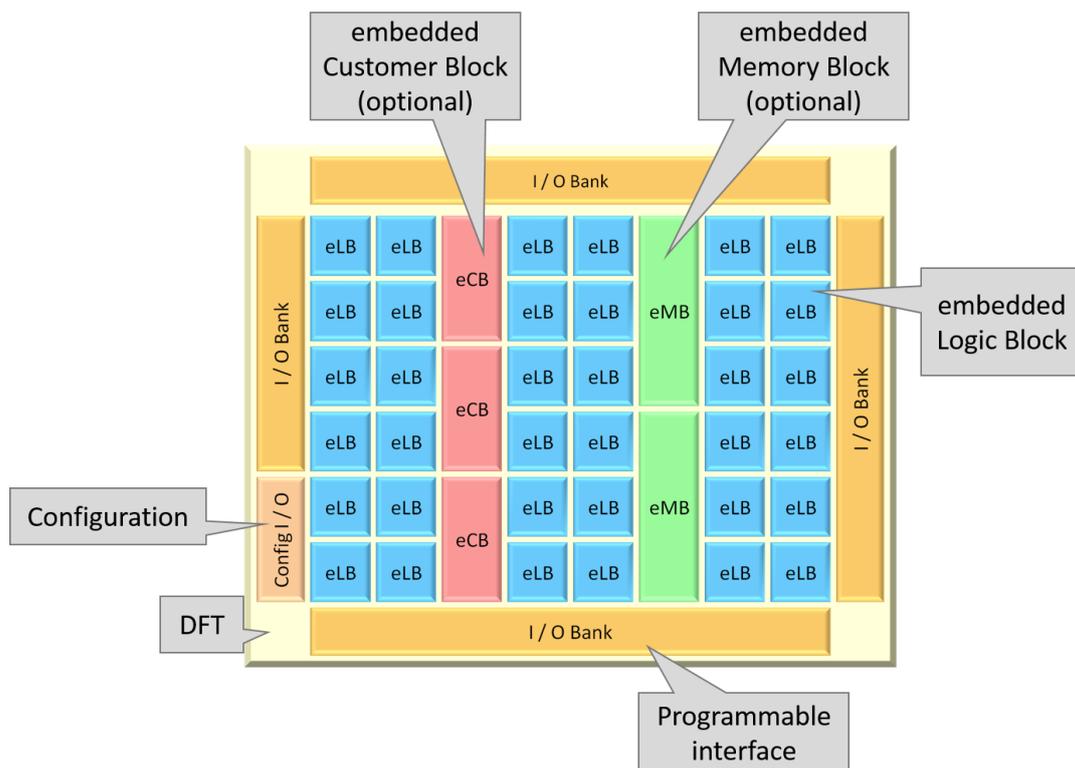
eFPGA Core IP architectural features

Key Benefits

- Designed specifically for SoC, ASIC or ASSP integration
- 4th generation of the architecture offering unmatched performances
- Highly customizable and scalable architecture
- Manufacturing DFT with full testability
- Versatile and easy to use application synthesis, mapping and place and route tools

Use cases

Menta eFPGA can be used to implement cryptography algorithms with added security and tunable post-manufacturing based on local regulations.

Often, it is necessary to tune digital radio filters after manufacturing through complex embedded software modifications or by adding a standalone FPGA. Menta eFPGAs allow implementation of circuitry including FIR filters, and tune them after manufacturing.

Architecture

The main building block of the eFPGA Core IP architecture is the eLB (embedded Logic Block). This configurable logic block is interconnected as an array using programmable routing resources. To support high-speed arithmetic functions, a hardwired carry chain is included that connects eLBs. Additional specific blocks (eCBs) can be inserted inside the array to increase performance for application-oriented design. This can be Menta 18bits DSP MAC or any customer block performing arithmetic operations. The Core IP can also include foundry memory (eMBs).

Custom Architecture

The eFPGA Core IP is scalable and customizable with Menta Origami Designer™. Configuration parameters include: number of eLBs, number and type of eCBs and eMBs, number of clocks, and number of IOs. The aspect ratio of the core can be tailored to obtain the optimum design fit within the SoC.

Configuration

The eFPGA Core IP supports serial or parallel buses for configuration. Interfaces are provided as soft IPs.

Manufacturing Test

The eFPGA Core IP features full DFT compatibility that widely relied upon ASIC test solutions. Menta IPMs offer test coverage of up to 99.8%.

Programming tool suite

Menta Origami Programmer™ encapsulates all the steps of a classical FPGA design flow with an intuitive graphical interface. Based on user IEEE RTL (VHDL, SystemVerilog or Verilog), chosen eFPGA architecture and SDC design constraints, Origami Programmer™ computes the programming bitstream file. The software also outputs speed estimations, as well as a model that can be used in standard simulation flow and for equivalence check.
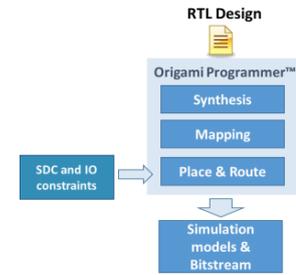
Origami Programmer™ design flow

Availability

The eFPGA Core IP can be ported to any CMOS process node within a few months.

Menta eFPGA custom Core IPs are readily available for TSMC 28HPM, STM 28FDSOI and GlobalFoundries 14LPP.

Pre-defined IP families, called IPMs, are ready for use in TSMC 28HPM and GlobalFoundries 14LPP. The IPMs range from 7k to 60k equivalent logic gates.

Performances

Physical implementation sample data for a 15k equivalent logic gates IP with DSPs.

	TSMC 28HPM	GF 14LPP
Eq. logic gates density (#/mm²)	20k	30k
Single stage max logic frequency (WC) (MHz)	740	1 770
Leakage power (mW) – 25°C, 0.9V, TT	0.5	0.6

For more information about Menta products, visit us on the web at: www.menta-efpga.com or contact info@menta-efpga.com