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Building Flexible SoCs

Menta eFPGA IP

THE Solution for Embedded FPGA

The reasons for embedded FPGA (eFPGA)

Protect your secrets. In today's global, multi-player design-chain, preserving IP/trade secrets is more critical and challenging than ever. There is no better strategy than withholding the "crown jewels" of your technology until your product is in your customers' hands. With Menta eFPGA you can wait to deliver your most proprietary technology to end-customers as a field-upgrade, minimizing any opportunity for competitors to reverse engineer your product.

Reduce development and life-cycle costs. At higher production volumes, on-board FPGAs quickly become cost-prohibitive. With Menta eFPGA you integrate on-board FPGA functionality *on-chip*, saving manufacturing costs and board-space, while fully maintaining field-upgradability. Similarly, if your company in the past has relied on SoCs, Menta eFPGA enables you to minimize the number of chip-variants, time-to-market, and dynamically adapt to evolving standards.

Higher performance. Standard FPGAs have been a classic solution for processor-acceleration, but engineers must deal with sacrifices in board-space, I/O latency, and bandwidth. With Menta eFPGA, those sacrifices disappear, as you bring those accelerators *on-chip*, without the limitations/overhead due I/O pad-count or chip-to-chip communication interfaces.

Embedded FPGA enables *flexible and secure* SoCs. Developing a typical system/SoC today costs $10M-$100M. Flexible SoCs ensure that you maximize the return on that investment.

Unparalleled process-portability Maximizing flexibility requires maximizing process-portability, not just across geometries but also different variants for low-power, high-speed, or even "rad-hard" space-applications. Menta eFPGA is the only 100% standard-cell based solution, while all our competitors use full-custom design

to various extents. Menta's standard-cell based approach enables rapidly porting your eFPGA to whatever new process geometry/variant you desire, using the same automated, standard EDA flow as for the rest of your SoC. Because they rely on custom-cells, competitors require several months to port their eFPGA to a new process, while Menta, using its industry gold-standard Synopsys-based implementation flow, enables portability within just weeks.

As a result of Menta's commitment to maximizing process portability, our eFPGAs have been silicon-proven on more technology nodes than any other eFPGA vendor. To date, Menta eFPGAs have been successfully manufactured on technologies as diverse as: STM130, STM65, TSMC 28HPC+ and GLOBALFOUNDRIES 14LPP. Menta eFPGAs are qualified on GLOBALFOUNDRIES® 32 SOI and 14LPP. Menta is also a

	Small		Medium	Large		XLArge		Dedicated
Feature	**M5S0.5**	**M5S2**	**M5M5**	**M5L15**	**M5L40**	**M5XL65**	**M5XL130**	**?**
# LC	596	1 605	4 815	14 884	40 128	65 664	130 000	?
# Adaptive DSP	0	6	11	24	60	25	1000	?
# Specific arithmetic block	-	-	-	-	-	-	-	?
SRAM (kb)	0	0	1 442	0	1 966	2 425	5 252	?
# IOs	667	844	1 388	3 436	3 808	4 770	6 500	?

eFPGA IPs examples 1 LC = 1 LUT4 + FF

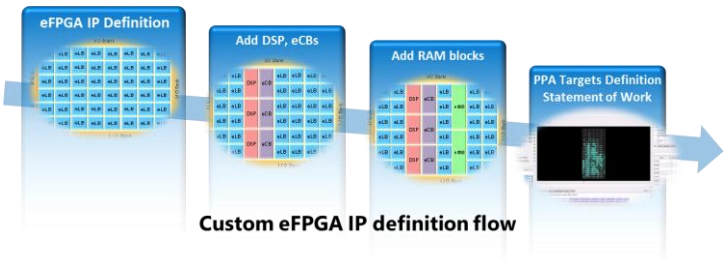
22 FDXcelerator™ Partner. Menta IPs are currently being delivered on XFAB 180nm, TSMC 12FFC and TSMC N6.

Customize your eFPGA, all the way from 100 to 200K Logic cells

Menta allows customers to specify the number of embedded Logic blocks (eLBs), number and configuration of adaptive DSP, RAMs, number/type of interconnects, as well as different power-saving features. The goal is to enable you to architect the exact FPGA you want to suit your needs.

Add adaptive DSP and eCBs

Menta offers designers an adaptive DSP logic block to incorporate within their eFPGAs. Designers can select the elements of the DSP such as using a pre-added or not. They can add Menta patented FIR engine which offers unmatched efficiency for signal processing, especially FIR/IIR filters. In addition, the adaptive DSP is entirely sizable to fit designers' requirements whether they need 8bits precision for AI inference or 48bits precision for high quality audio. Designers can even embed their own proprietary arithmetic logic blocks (eCB).

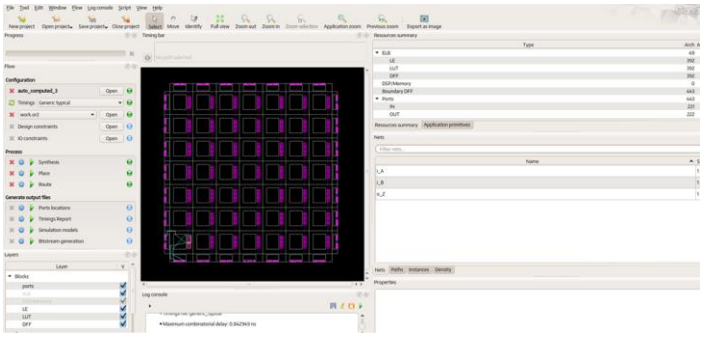


Custom eFPGA IP definition flow

Program your eFPGA – with Origami Programmer

Like all top FPGA vendors wanting to ensure best possible results, Menta created a specially "targeted" programming software-tool, Origami Programmer, to generate the bitstream that targets/optimizes your RTL specifically to the Menta eFPGA architecture. Menta does not rely on 3rd party software tools which target "generic" FPGA architectures, thus delivering suboptimal results. Finally, Menta's independent software development frees Origami Programmer from any export-control and patent litigation issues.

After development, bitstream loading using Origami Programmer is very similar to the way you would program a traditional synchronous memory using a 16-bit wide address-bus.



Easy to integrate and verify within the rest of your SoC design

It is essential that any IP, whether flexible or not, must never put the remainder of the SoC at risk. For this reason, Menta designed its eFPGA so that it can be verified at various levels: using formal verification for mapped applications, system simulation with SDF timing information, and even gate-level simulation post place-and-route. Bitstream loading can be simulated and verified as well. We call it *Trusted eFPGA*.

Register-based bitstream to fully ensure testability

Because of the major investment required to develop modern SoCs, testability is key. Menta eFPGA IPs offer full compatibility and easy integration with all of the most common ASIC DFT solutions. Menta IPs use 100% flip-flop based patented DFT structures, with a multiplexed scan approach. Scan compression structures and boundary scan wrappers are inserted to enable the best possible test-efficiency and complete isolation of the IP from any surrounding logic.

Menta provides test patterns in different formats (STIL, WGL) and types (SAF, TFT). ATPG patterns are validated at gate-level in the signoff corners DFT structure insertion and the ATPG flow are performed using Synopsys tools (DFT Compiler, DFTMAX, TetraMAX). We achieve a test coverage in excess of 99.8%.

Well capitalized

Menta is backed by FJ Development EN, with an investment of more than $7M to date.

Datasheets, Menta Starter Pack training & evaluation software on any process node, as well as TSMC 28HPC+ evaluation board are available. For more information visit our website at: www.menta-efpga.com

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